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The development and test research of a multichannel synchronous transient electromagnetic receiver

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Abstract. As a result of the drastic reduction in shallow mineral resources, the exploitable potential and reserves of proven mines are insufficient, and the mineral resources in deep ground need to be more explored in a more refined way. There are some disadvantages of the existing instruments, such as few channels and slow sampling rate. Therefore, a multiparameter transient electromagnetic instrument with synchronous receiving has been developed and tested. The instrument is composed of two controllers - embedded controller and programmable logic controller - which can provide a diversified information combination for follow-up information processing. Under the grounding electrode source emission mode, the real-time synchronous transient electromagnetic acquisition system of six channels is achieved with a sampling rate of 128000 samples per second (SPS). The data acquired by the six channels is recorded in the full-time range of the time domain. Furthermore, experiments were carried out in the laboratory, open areas, and actual mine. Through data analysis, the measured data curves of the mining area are highly consistent with the existing geochemical exploration curves and geological profile.

1 Introduction

The transient electromagnetic method (TEM) belongs to the active field source method of time domain electromagnetism. James R. Wait first proposed the transient electromagnetic method to search for conducting ore bodies in 1951. In recent decades, TEM receivers have been widely used in

metal mineral, petroleum, and natural gas exploration and other fields (Danielsen et al., 2003; Haroon et al., 2015), so many kinds of TEM receivers have been developed and manufactured (Li et al., 2012), such as the V8 receiver from Phoenix Geophysics (Phoenix Geophysics, 2017), ADU-07e from Metronix (Metronix, 2017), and KMS-820 from KMS (KMS, 2017), which are easy to use and have good performance. Meanwhile, the TEM detection theories have also been developed (Wright, 2004). In 2010, the internationally renowned geophysicist Zhdanov proposed the following directions for future electromagnetic exploration instruments and methods at the 75th Annual Conference of Geophysics: multicomponent emission, multichannel reception and pseudo-seismic data collection (Qi et al., 2015; Ayuso et al., 2016). Xue Guoqiang proposed the short offset transient electromagnetic method (SOTEM) (Xue et al., 2013; Chen et al., 2016, 2017), and the reduction in transceiver distance can both greatly enhance the exploration depth and improve the signal-to-noise ratio (SNR). Because of the demand for increased exploration depth and the need to obtain more diverse subsurface geological information, the number of channels, high SNR, and synchronization are the key elements for TEM receiver development, which are useful for obtaining more abundant underground geological information and improving the accuracy of detection. Therefore, we propose a multichannel synchronous transient electromagnetic receiver, which has the characteristics of multichannel synchronous parallel acquisition, a large-capacity (64G) storage with full-time synchronization, and a sampling rate



Figure 1. System block diagram of hardware.



Figure 2. INA114 instrument amplifier and programmable gain amplifier circuit.

of up to 128 000 SPS, while the sampling rate of the V8 receiver is 96 000 only.

The main purpose of this paper is to introduce a receiver system for the synchronous acquisition of multiple electromagnetic signals in transient electromagnetic prospecting to achieve multiparameter and multichannel synchronous reception. High-speed programmable logic devices are used to achieve high-level synchronization between different channels. Transmitting current waveform acquisition and multichannel reception can be synchronized by using a highprecision Global Position System (GPS) timing unit which is controlled by a serial port of microcontroller, and a highprecision counter is used to further improve the synchronization of data acquisition, especially when multiple receivers work in distributed mode (X. H. Zhang et al., 2017).

2 Multichannel receiver hardware and software design

2.1 Receiver framework

The receiving system consists of four parts, namely a field programmable gate array (FPGA) unit, an advanced reduced instruction set computer (RISC) machine (ARM) unit, an

Table 1. Magnification test of six channels.

Channel no.	Magnification mean value
Channel 1	94.42
Channel 2	94.46
Channel 3	94.39
Channel 4	94.68
Channel 5	94.32
Channel 6	94.59

analog acquisition unit, and a power supply circuit. The system block diagram is shown in Fig. 1. The numbers of analog boards are marked as channels 1/2, 3/4, and 5/6, and each board has two channels. The board contains the signal-conditioning circuit and channels for amplification and acquisition, which are completely independent. Hence, multichannel real-time synchronized acquisition is achieved.



Figure 3. AD5272 digital potentiometer.



Figure 4. DAC7714 potential compensation and reference voltage circuit.

2.2 Design of analog circuit board

The analog board mainly includes the signal conditioner (including the first-stage instrumentation amplifier, the secondstage programmable amplifier, and a low-pass filter), a protection circuit (input stage clamp diode), the natural potential compensation circuit (Liu et al., 2016), a single-endedto-differential circuit, and an analog-to-digital converter.

The first-stage amplifier uses a dedicated high-precision, low-noise amplifier INA114, and a high-resolution digital potentiometer AD5272 is used to design the precision gain op-amp to achieve high-precision amplification and range adjustment. The two circuits are shown in Figs. 2 and 3.



Figure 5. Single-ended-to-differential converter circuit.



Figure 6. Analog-to-digital converter circuit.

In Fig. 2, the circuit utilizes the programmable gain amplifier PGA103 and a general input and output (IO) port to complete the three-level amplification ratio adjustment.

Two natural potential compensation voltages and two fullscale reference voltages are supplied by DAC7714, a 12 bit digital-to-analog converter with four output channels. The DAC7714 circuit is shown in Fig. 4. The multichannel receiver has a wide input voltage range, which varies from -5 to +5 V, and the amplitude of the signals actually collected is from dozens to hundreds of millivolts. ADA4941 is a single-ended-to-differential converter that is used as the front part of an analog-to-digital converter. Each channel of the receiver uses a separate AD7767, a 24 bit high-resolution and wide dynamic-range converter. The AD7767 is a $\sum -\Delta ADC$ with oversampling characteristics, which can reduce noise from the front end and the need for a front-end anti-alias filter, and uses its daisy chain technology to realize the multi-chip cascade connection for an efficient parallel synchronous acquisition method (Liu et al., 2017). These two circuits are shown in Figs. 5 and 6.

	U3		<u>R10</u>
DREADY21	IO L 22NI VIDEE 2	IO I 1D USWADEN O	
	IO L83N_VKEF_3	IO_LIP_HSWAPEN_0 IO_LIN_VREF_0	143 DREADY5
$100R \frac{\text{GND}}{100R} \frac{\text{GND}}{1223V} \frac{3}{4}$	GND	IO L2P 0	142 DREADY3
$\pm 3.3 \text{ V} = 4$ DRFADV15	VCCO_3	IO_L2N_0	140 DREADY6
SDI1 6	IO_L52N_3	IO_L3P_0	139 SRA17
SDI2 7	IO_L52P_3	IO_L3N_0 IO_L4P.0	138 SRA16
<u>SDI3</u> 8	IO L5IP 3	IO_L4I_0 IO_L4N_0	137 SRA15
SYNC 9	IO L50N 3	GND	136 GND 125 12 2V
MCLK 11	IO_L50P_3	VCCO_0	135 +5.5V 134 SR/OE
CS 12	IO_L49N_3	IO_L34P_GCLK19_0	133 SR/UB
<u>GND 13</u>	GND	IO_L34N_OCLK18_0 IO_L35P_OCLK17_0	132 SR/LB
CHI A3 14	IO L44N GCLK20 3	IO L35N GCLK16 0	<u>131 SRI/O15</u>
CHI AL 16	IO_L44P_GCLK21_3	GND	129 +3 3V
PPS TRIG 17	IO_L43N_GCLK22_IRDY2_3	VCCAUX	128 +1.2V
+3.3V 18	10_L43P_GCLK23_3	IO I 36P CCLN1	127 SRI/O14
+1.2V 19	VCCINT	IO L36N GCLK14 0	126 SRI/013
+3.3V = 20	VCCAUX	VCCO_0	$\frac{125 + 3.3V}{124 \text{ SPI/O12}}$
CH2 A2 22	IO_L42N_GCLK24_3	IO_L37P_GCLK13_0	124 SRI/012 123 SRI/011
CH2 A1 23	IO_L42P_GCLK25_TRDY2_3	IO_L3/N_GCLKI2_0	122 +3.3V
CH2 A0 24	IO L4IN_GCLK20_3	IO L62P 0	121 SRI/O10
GND 25	GND	IO L62N VREF 0	120 SRI/O9 110 SPI/O8
CH3 A3 27	IO_L37N_3	IO_L63P_SCP7_0	119 SRI/08
+1.2V 28	IO_L37P_3	IO_L63N_SCP6_0	117 SRA13
CH3 A2 29	IO L36N 3	IO_L64N_SCP3_0	116 SRA12
<u>CH3 A1 30</u>	IO L36P 3	IO L65P SCP3 0	115 SRA11
$\frac{+5.3 \vee -31}{CH3}$ A0 32	VCCO_3	IO_L65N_SCP2_0	114 SKATU 113 GND
CH4 A3 33	IO_L2N_3	GND IO L 66D SCDL 0	112 SRA0
CH4 A2 34	IO LIN VREF 3	IO_L66N_SCP0_0	111 SRA1
<u>CPU RESET 35</u>	IO_L1P_3	TDI	110 FPGA TDI
$\frac{\pm 3.3 \times 30}{\text{FPGA PROG B} 37}$	VCCAUX	TCK	109 FFGA TCK
SPI CS N 38	PROGRAM B 2	GND	107 FPGA TMS
FPGA INT B 39	IO L65P INIT B 2	TDO	106 FPGA TDO
<u>CH4 AI 40</u>	IO_L64N_D9_2	IO_L1P_1	105 SRA2 104 SP A3
+3.3V 42	IO_L64P_D8_2	IO_L1N_VREF_1	103 +3.3V
CH5 A3 43	VCC0_2 IO L 62N D6 2	VCCO_I IO_I_32P_1	102 SRA4
<u>CH5 A2 44</u>	IO L62P D5 2	IO_L321_1 IO_L32N_1	101 SR/CE
CH5 A0 46	IO_L49N_D4_2	IO_L33P_1	100 SRI/O0 99 SRI/O1
CH6 A3 47	IO_L49P_D3_2	IO_L33N_1	98 SRI/O2
CH6 A2 48	IO_L48N_RDWR_B_VREF_2	IO_L34P_I IO_L34N_1	97 SRI/O3
GND 49	GND	GND	<u>96 GND</u>
<u>CH6 AI 50</u>	IO_L31N_GCLK30_D15_2	IO_L40P_GCLK11_1	<u>95</u> <u>SRI/04</u> 94 <u>SRI/05</u>
+1.2V 52	IO_L31P_GCLK31_D14_2	IO_L40N_GCLK10_1	93 SRI/06
+3.3V 53	VCCAUX	IO_L4IP_GCLK9_IRDYI_I	92 SRI/07
GND 54	GND	GND	91 GND
<u>ΓΡΟΑ ΟULKI 55</u> DΔT2 56	IO_L30N_GCLK0_USERCCLK_2	VCCAUX	$\frac{90}{89}$ $\frac{+3.3}{12}$
DAT3 57	IO_L30P_GCLK1_D13_2	VCCINT	88 SR/WE
CMD 58	IO_L14N_D12_2 IO_L14P_D11_2	IO_L42P_OCLK/_I IO_L42N_OCLK6_TRDV1_1	87 SRA5
SDP4 59	IO_L13N_D10_2	VCCO 1	86 +3.3V
CLK 61	IO_L13P_M1_2	IO_L43P_GCLK5_1	84 SRA7
DATO 62	IO_L12N_D2_MISO3_2	IO_L43N_GCLK4_1	83 SRA8
+3.3V 63	VCCO 2	IO_L45F_1 IO_L45N_1	82 SRA9
SPI DIN 64 FPGA MISO 65	IO_L3N_MOSI_CSI_B_MISO0_2	IO_L46P_1	81 SPIL NSS 80 SPIL SCLK
DAT1 66	IO_L3P_D0_DIN_MISO_MISO1_2	IO_L46N_1	79 SPI1 MISO
67	IO_L2N_CMPMOSE_2 IO_L2P_CMPCLK_2	IO_L47P_1 IO_L47N_1	78 SPI1 MOSI
GND 68	GND	GND	77 GND
FPGA_MU69 SPL_CLK70	IO_L1N_M0_CMPMISO_2	VCCO_1	<u>75 (</u>
FPGA DONE 71	IO_LIP_CCLK_2	IO_L74P_AWAKE_1	74
72	CMPCS B 2	IO_L/4N_DOUT_BUSY_I SUSPEND	
	VC6SI V0	5051110	$1 \frac{10K}{10K}$
	ACUOLAY		
+5.3V			

Figure 7. FPGA controller unit circuit.



Figure 8. STM32F407 unit circuit.

Table 2. Error analysis of interchannel consistency.

Channel no.	Group 1 (mV)	$Group\ 2\ (mV)$	Group 3 (mV)	Group 4 (mV)	Average (mV)	Average error (mV)	Error percentage (%)
Channel 1	20.7398	20.7372	20.7382	20.7359	20.7378	0.0020	0.1901
Channel 2	21.0451	21.0465	21.0510	21.0465	21.0473	0.0022	0.3432
Channel 3	20.7961	20.7927	20.7938	20.7964	20.7948	0.0013	0.1328
Channel 4	21.0050	21.0044	21.0057	21.0015	21.0042	0.0008	0.2303
Channel 5	21.0529	21.0504	21.0500	21.0530	21.0516	0.0013	0.0282
Channel 6	20.8906	20.8911	20.8906	20.8914	20.8909	0.0004	0.2013

By adopting a modular design, two AD7767 chips are cascaded, and an FPGA controller is used to control the three analog circuit boards separately, and therefore the overall data packaging and storage in real time is achieved. The AD7767 chip has a maximum output data rate of 128 kHz, so the bandwidth of the receiver ranges from direct current (DC) to 12.8 kHz. For a good accuracy of collection, the frequency of the input signal should be less than 12.8 kHz.

2.3 Design of the digital logic controller board

The multichannel synchronous receiver is made up of an embedded controller and an FPGA controller (Oballe-Peinado et al., 2017), which is flexible and widely used. The FPGA is the core controller of the receiving system, and the synchronization between the various functional units can be easily achieved by its parallel processing function; therefore, a number of logic modules are driven by the same clock source. This receiver uses an XC6SLX9 chip as the core acquisition controller, that belongs to the Spartan-6 series of the well-known FPGA chip maker Xilinx. It is shown in Fig. 7. The FPGA unit is mainly composed of an SD card unit circuit, static random access memory (SRAM) buffer circuit, and the serial peripheral interface (SPI) which is used to communicate with the STM32 controller, the synchronous signal acquisition and control interface of six channels, and GPS's pulse per second (PPS) signal interface and power interface.

The STM32F4 series of ST Microelectronics is adopted as controller unit which is popular in industry and instrumentation. The embedded controller unit has the following func-

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Figure 9. High-precision power circuit.

tions: keyboard input, communication with the FPGA, GPS location information collection, and a liquid crystal display (LCD). The collected GPS information is composed of latitude, longitude, time, and so on, which is output by the GPS module through the serial port and simultaneously displayed on a LCD. A 6×8 matrix keyboard is designed to set the system parameters and select the channel for data collection. When the GPS satellite signal is locked, the receiving system can collect the data according to the preset instruction by a start key. A general-purpose IO port is used to control the DAC7714 chip to achieve natural potential compensation, reference voltage, and fine gain tuning. The STM32F407 diagram is shown in Fig. 8.

2.4 High-precision linear power circuit

Low-dropout–output linear power chips with a highprecision and a high ripple rejection ratio are selected (Joo et al., 2017; Duong et al., 2017). On the power board, there are three independent connecting plugs connecting each analog board (Ren et al., 2015). In the receiver, the TPS7A series chips are selected, which are manufactured by the Texas Instrument company. These chips have the following characteristics: a wide input voltage range, low noise, and a high ripple rejection ratio. The power board has four different output voltages (+10, -10, +5, and -5V), which are used for preamplifiers and the programable gain amplifier (PGA). Another separate +5V power supply for the digital potentiometer on the analog board and the DAC7714 chip and 3.3 V power provide digital logic power for the analog-to-digital converter AD7767 (Yun et al., 2017). The power diagram is shown in Fig. 9. Since all chips are low-powered, the overall power consumption of the receiver is less than 10 W.

2.5 Software design

The software mainly includes two parts: (1) the program of the FPGA unit, which involves the data storage on an SD card, real-time communication with STM32, data processing in data buffer area, and so on; (2) the program of the STM32 unit, which includes the gain adjustment of the first-stage preamplifier, the ratio setting of the second-stage programmable amplifier, and natural potential compensation control (Khomutov et al., 2017).

The FPGA mainly controls the front-end analog-to-digital converter, data storage, and interactions with STM32 by SPI.



Figure 10. Flowchart of system program.



Figure 11. The relation of input signal amplitude and amplification ratio in DC testing.

First, the FPGA controller loads the program from flash after power-on and then waits for the operation control commands sent from STM32, such as system initialization, parameter setting, and sensor calibration (Wang et al., 2017). Time information and the channel serial number are stored on an SD card through the FPGA program. The information is stored



Figure 12. Sine waveforms received by six channels synchronously.



Figure 13. Waveform and its spectrum diagram.

in the first 8 bytes in each sector of the SD card. The PPS provided by the GPS unit is used to update the internal base time of the FPGA every 2 s. It can reduce the time cumulative error.

The embedded controller is responsible for coordinating the operation of the entire system, such as the system gain adjustment of each channel, GPS time information reception and status monitoring, and real-time display of acquired data, and communicating with the FPGA controller (X. Y. Zhang et al., 2017). The system flowchart is shown in Fig. 10.

3 Performance testing

Performance testing of the receiver system mainly includes DC testing, AC testing, and field testing (Ziolkowski et al., 2010; Zhou et al., 2015). In the DC stability testing, we first tested the magnification range of each channel and the magnification consistency. Taking the first channel as an example, as is shown in Fig. 11 below, the input signal is a blue curve with a range of \pm 50mV. The green curve is the mag-



Figure 14. Background noise of receiver.



Figure 15. Single cycle waveform (40 ms).

nification times of the first channel when each data value of input signal was calculated. Under the same test conditions, the six channels were connected in parallel, and the same input signals were received separately by six channels at the same time. The average magnification times of each channel are shown in Table 1.

Next was the conformance test for channels of the receiver. The test aimed to confirm high consistency between channels. In the test, the positive terminals of the six channels were connected together as a positive port, while negative terminals were linked to each other as a negative port. The two ports were input with standard sine waves. The peak-to-peak voltage value of input signal was 20 mV and its frequency was 150 Hz. The extracted numerical values of each channel at the same time were compared to obtain the average error, the average absolute error, and error percentage, as is shown in Table 2. The average error is less than $2.2 \,\mu$ V.



Figure 16. Profile of the open area.



Figure 17. Waveform diagram of data collected in mining area.

In the AC testing, the six channels of the positive and negative terminals were connected separately, and the sine waves generated by a standard signal generator were input to the receiver. The waveforms generated by the collected data are shown in Fig. 12. The peak-to-peak value of the input signal was 10 mV, and its frequency was 20 Hz. As can be seen from the figure, the consistency between each channel is quite high and there is no phase offset. After the input signals are amplified by a two-stage amplifier in the analog board, the output peak-to-peak value of each channel is up to 1000 mV.

$$SNR = 20 \times \log \frac{\text{full scale value}}{\text{root mean square value of noise}}$$
(1)

Figure 13a shows the waveform of three cycles of data acquired by the first channel shown in Fig. 12. Figure 13b presents the frequency spectrum formed by fast Fourier

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Figure 18. Survey line profile of mining area.



Figure 19. Anomaly of geochemical exploration of mining area along the survey line.

transform (FFT). As is shown in Fig. 13b, the frequency of the input sine waves is 20 Hz, and the frequency spectrum has few harmonic components, which indicates the excellent performance of the analog circuit board and the high stability of the power circuit.

In Fig. 14, when six channels are connected to zero voltage in the same way, 2000 data points of each channel are displayed. According to Eq. (1), the SNR of each channel is calculated to be approximately 100 dB.



Figure 20. Geological profile of mining area.



Figure 21. Receiver.

4 Field testing

In field testing, a hollow coil with 400 turns and a diameter of 50 cm was used as the receiving sensor (Brunke et al., 2017), and its effective area is 40 m^2 . Phoenix T-4 transmitter is a small power transmitter, which is manufactured by Phoenix. This transmitter can launch up to 40 A currents, powered by a battery group, and it can launch many kinds of waveforms, such as TD50 (numbered by Phoenix), which is a bipolar pulse waveform with a 50% duty cycle (Wang et al., 2015) and was used in the actual test. The V8 system is the eighth generation of receiver technology developed by Phoenix since 1975. The V8 sampling rate is 96 000, and its flash memory capacity is 512 MB only. It cannot store all received data and is synchronized by a GPS unit. However, the



Figure 22. T4 transmitter.

sampling rate of the multichannel TEM receiver is 128 000 SPS, and the synchronization mechanism is realized by GPS and a 28 bit high-precision counter. The accuracy of synchronization can be improved, and all the time information and collected data are stored on an SD card simultaneously.

Two sites were selected for field testing, one of which is a relatively open area; the other is the actual mining area. The near-field measurement method was used in the test. A grounded electrode source was adopted as the field source. Four aluminum plates were used as electrodes, which were linked together and buried 40 cm deep in the ground and covered with saltwater and soil, so that the grounding resistance was less than 10Ω . The distance between the transmitting electrodes A and B was 400 m, and four batteries were used as the power supply. The voltage ranged between 40 and 50 V. The emission current was 3 A, and the emitting frequency was 25 Hz.

During the test, the power supply electrodes were stationary, while the preset measurement line was parallel with the transmitting line. The offset between transmitting line and receiving line was 40 m. The changing rate of the magnetic flux density (dB / dt) was received by the coil. Figure 15 below shows one original cycle.

The open area where the test was carried out is formed by the mixture of soil and building slag. The measurement line was observed at eight measuring points. After the data was stored, data of the eight collecting points were processed by a MATLAB computer program. Then, the secondary field information of each testing point was extracted. The resulting profile curve was formed.

Figure 16 shows the profile, which is formed by the extracted data and indicates that the overall response tends to be flat. The signals received at the measurement points close to the transmitting nodes are relatively strong, while the central part of the profile becomes flat slowly.

In order to test the performance of the receiver further, a mining area in Leshan, Sichuan Province, China, was selected for the field test, and a relatively gentle geodetic survey line was planned. The electrode source emission was adopted, and the distance between the transmitting electrodes was 400 m. The testing line offset was 80 m, and the distance between the measuring points was 40 m.

A continuous launch mode was used in a mining area test, and the transmitting frequency of the signal was 25 Hz. A multichannel synchronous transient electromagnetic receiver can be used to collect the data of the transmitting current waveform, the change rate of the magnetic field, and the intensity of the electric field.

Figure 17 is composed of three sub-figures in the mining area. Figure 17a shows the change rate of the magnetic field (dB / dt), and Fig. 17b presents electric field intensity; Fig. 17c is about the transmitting current waveform. All subfigures display two periods of signals (80 ms). Figure 17a and b were formed from data acquired by a receiver, and Fig. 17c was formed from data acquired by another receiver. The high-precision synchronization mechanism is implemented with a high-reliability GPS module and a 28 bit counter in the FPGA. The receiver's time information is refreshed every 2s by the PPS of the GPS module. The 28 bit counter is used to record the pulses, which come from a 25 MHz clock in an FPGA chip. The 28 bit counter value, time information, and data collected by the receiver are packaged and stored on an SD card. The time error between every two points is 40 ns according to the period of the 25 MHz clock and the frequency of refreshment. Each collected sample can be tracked by the stored time information and data information on an SD card. The full-time range storage technology can greatly enhance the synchronization accuracy, even with many receivers working at the same time in the mining area.

The acquired data in the mining area were second-field extracted, filtered, and interpolated, and the waveform was formed. The waveform of the time domain is smoother after waveforms were superimposed 200 times, which can reflect the response of underground geological bodies to TEM well. The data of each measuring point were processed to obtain the pure secondary field curves, and the time domain waveforms were extracted to form the profile of the measuring line. In Fig. 18, t1-t12 represent the extraction time (Zhong et al., 2016), and the extracted values of different collection points were collected together to form 12 curves at different time points.

As can be seen by comparing Figs. 19 and 20 with Fig. 18, the high anomaly point is near Point 1160, which happens



Figure 23. The mining area map.

to be a sloped metal vein. Thus, it is verified that the receiver can acquire signals of transient electromagnetic emission very well. By analyzing and comparing the profile with the actual geochemical distribution, it can obviously be seen that the abnormality of the curves is highly consistent at Point 1160. In addition, the anomaly is consistent with the geological structure in this area. Figure 21 is the receiver photo, and Fig. 22 shows the T4 transmitter working at the testing field, and Fig. 23 is the map of mining area.

5 Conclusions

The purpose of this paper is to develop the multichannel synchronous receiver that can be applied in transient electromagnetic prospecting. First, the hardware circuits and software programs were designed to realize the functions mentioned above. By means of a dual controller, the receiver can acquire signals synchronously through six independent channels. Then, the data stored on an SD card were processed by computer programs to generate profile graphs. The overall performance of the receiver was tested and verified. All the collected data error of each channel is less than 0.35 %, and each channel can connect different sensors, such as coils, magnetic probes, and electrodes. The receiver can be used to collect transient electromagnetic information. Due to its high precision and high sampling rate, it can capture the fast falling edge of TEM and ultralow noise and so on. Hence, by adopting the receiver, the multichannel synchronous acquisition of magnetic field information in three directions, electric field information in two directions, and the changing rate of magnetic induction intensity can be realized in the time domain reception.

In addition, the reliability, practicability, and data validity of the receiver were verified by field testing in the mining area. Meanwhile, the receiver can be used for pseudorandom signal reception and distributed three-dimensional data reception, which can improve geophysical exploration efficiency.

Code availability. The codes of the receiver are available upon request (linfq@cdut.edu.cn).

Data availability. The circuit schematics of the receiver are available upon request (linfq@cdut.edu.cn).

Author contributions. FQ developed the main hardware and part of the software, and XB instructed all the authors. The other authors participated in the experiments and software development.

Competing interests. The authors declare that they have no conflict of interest.

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